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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER

KIM, H

ART UNIT

PAPER NUMBER

2185

DATE MAILED:

02/01/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

08/984,563

Applicant(s)

Mailloux et al.

Examiner

H. Kim

Group Art Unit

2185

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE _____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- ☒ Responsive to communication(s) filed on 10/23/00
- ☐ This action is **FINAL**.
- ☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- ☒ Claim(s) 36-39 + 59-74 is/are pending in the application.
- Of the above claim(s) _____ is/are withdrawn from consideration.
- ☐ Claim(s) _____ is/are allowed.
- ☒ Claim(s) 36-39 + 59-74 is/are rejected.
- ☐ Claim(s) _____ is/are objected to.
- ☒ Claim(s) 70-74 are subject to restriction or election requirement.

Application Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
- ☐ received.
- ☐ received in Application No. (Series Code/Serial Number) _____.
- ☐ received in this national stage application from the International Bureau (PCT Rule 1.7.2(a)).

*Certified copies not received: _____

Attachment(s)

- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____ ☐ Interview Summary, PTO-413
- ☒ Notice of References Cited, PTO-892 ☐ Notice of Informal Patent Application, PTO-152
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948 ☐ Other _____

Office Action Summary

Detailed Action

1. Claims 36-39 and 59-74 are presented for examination. This office action is in response to the Amendment filed on 10/23/00.
2. It is noted that this application appears to claim subject matter disclosed in the co-pending section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending applications to avoid possible double patenting.

Restriction

3. Newly submitted claims 70-74 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: WCBR, instructing the asynchronous DRAM a desired memory operation, and performing the desired memory operation until terminated were not originally claimed.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 70-74 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

DOUBLE-PATENTING

4. The non-statutory double patenting rejection, whether of the obviousness-type or non-

obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman*, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claim 66 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 51, 59, 63, 64, and 67 of copending Application No. 08/984,561. Although the conflicting claims are not identical, they are not patentably distinct from each other because both sets of claims are related to a method of accessing a storage device, comprising: maintaining a first enabling signal in an active state, selecting burst and pipelined mode, receiving an initial external address, selecting read and write

operation, cycling a second enabling signal, generating an internal address, switching the mode of operation to a pipeline mode. Both sets of claims recited similar inventive concept of accessing a memory in burst and pipelined mode except: Claim 66 of the present invention comprises less element than as claimed in the Application No. 08/984,561. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to delete additional limitation of maintaining a first enabling signal in an active state of the copending application to arrive invention of the present application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

6. claims 70 and 74 are objected to because of the following informalities:

As to claim 70, it appear that an acronym "WCBR" should be changed to -- Write CAS before RAS (WCBR)-- for clarity.

As to claim 74, it is unclear what is meant by "generating includes iterating the act of generating until terminated". It appear that a phrase is missing after "act of generating".

7. Claims 36, 68, and 69 are objected to under 37 CFR 1.75(b) as not substantially differing from each other.

The claims as written do not appear to be substantially different or to provide substantially

different patent protection.

Applicants are required to 1) cancel the objected to claims,(2) amend the claims so that they are substantially different from any other claims, or (3) provide sufficient reasons why the claims as presently written are substantially different or provide substantially different patent protection.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. Claims 73 and 74 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It appears that there is no support for obtaining an external column address so as to perform the desired memory operation, and wherein performing includes iterating the act of obtaining the external column address until terminated and generating an internal column address so as to perform the desired memory operation, and wherein generating includes iterating the act of generating until terminated at the time the application was filed.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

10. Claims 36-39 and 59-62 are rejected under 35 USC 102(e) as being anticipated by *Manning*, U.S. Patent 5,610,864.

As to claim 59, *Manning* discloses a method of accessing a memory (Fig. 1), comprising: receiving an external row address (Fig. 1 and Fig. 2, ADDR, ROW); choosing whether the memory is in burst (col. 6 lines 14-26 and col. 7 lines 43-54) or a pipelined mode of operation (col. 5 lines 43-50); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); and executing a read or write operation (Fig. 2, /WE).

As to claim 60, *Manning* further discloses switching between a burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipeline mode (col. 5 lines 43-50).

As to claims 61, *Manning* further discloses switching between a read and a write operations (Fig. 2 /WE).

As to claim 62, Manning further discloses the operations are performed in a different order (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+).

As to claim 36, Manning discloses the invention as claimed. Manning discloses a method for accessing an asynchronously access memory (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16), comprising the steps of: receiving an external row address to the asynchronously accessible dynamic random access memory accessible storage device (Fig. 1 and Fig. 2, ADDR, ROW); selecting between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 43-50); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); obtaining a first external column address (Fig. 1 and Fig. 2, ADDR, COLm).

As to claim 37, Manning further discloses the step of obtaining a second external column address subsequent to the first external column address for operation in the pipeline mode (col. 5 lines 43-45)

As to claims 38, Manning further discloses generating internal address (col. 5 lines 51-62 and col. 8 line 67).

As to claims 39, Manning further discloses selecting path way (Fig. 1 Ref. 40 and col. 3

lines 20-22, col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 63-69 are rejected under 35 USC § 103(a) as being unpatentable over Manning, U.S. Patent 5,610,864 in view of Ryan, U.S. Patent 5,966,724 or Rosich et al. (Rosich), U.S. Patent 5,587,964.

As to claim 65, Manning discloses a method of operating a memory circuit, comprising: receiving a mode select signal(col. 6 lines 14-34); receiving an initial external address (Fig. 1 and Fig. 2, ADDR); selecting a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); cycling a second enabling signal (Fig. 2 /CAS) ; generating an internal address (Fig. 1 Ref. 26); and receiving an external address on each cycle of the second enabling (col. 5 lines 43-49, "one access per cycle" read on this limitation). Although

Manning discloses changing the mode and pipeline mode and, Manning does not specifically disclose a step of changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state.

Ryan discloses the step of changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state (Fig. 6, RAS and col. 8 lines 30-33) and receiving an external address on each cycle of the second enabling signal (Fig. 6 Ref. Addr) because it would allow the memory to switch mode of operation instantly thereby put the memory in high data throughput by eliminating the set up time (abstract lines 8-9).

One skilled in the art would have realized that maintaining a first enabling signal in active state would allow that the memory is always in ready to switch mode of operation thereby increasing the access speed of the memory.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the step of changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state of Ryan in the invention of Manning because it would allow the memory to switch mode of operation thereby increasing the memory access speed. The advantage of increasing the memory speed provide sufficient suggestion and motivation to one of ordinary skill in the memory art to follow the teaching of Ryan into invention of Manning.

Alternatively, Rosich discloses the step of changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state (col. 8 lines 24-48

and RASL in Fig. 7, Ref. 700, page mode & 710, burst mode) for the purpose of reducing memory access time and component latency by enabling the memory chip throughout the operations (col. 1 lines 21-31).

One of ordinary skill in the art familiar with Manning, and looking at Rosich would have recognized that the memory access cycle of Manning would have been reduced by maintaining a first enabling signal in active state during mode of operations because it would provide capability of that the memory is always in ready to receive a mode command thereby increasing the access speed of the memory. Increasing memory speed would have a highly desirable feature in the computer system environment of Rosich because the objective of computer system is increasing speed or computing power.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the step of maintaining a first enabling signal in active state of Rosich in the invention of Manning because it would increase memory access speed of Manning by providing capability of that the memory is always in ready to receive a command.

Rosich further discloses switching the mode select signal to select a first mode while maintaining the first enabling signal in the active state and changing the mode select signal to select a second mode (col. 8 lines 24-48 and Fig. 7, Refs. 700 & 710).

As to claim 66, Manning, Ryan, and Rosich disclose the claims as the above claim 65. Manning further discloses a step of maintaining a mode select signal to select a burst mode of

operation (Fig. 2 /OE, col. 7 lines 45-55 & col. 6 lines 14+) and switching the mode to a pipelined mode on successive cycles of the second enabling signal by changing the mode select signal (col. 5 lines 43-49, "one access per cycle" read on this limitation). Ryan and Rosich discloses a step of switching the mode on the successive cycles of the second enabling signal (Fig. 6, RAS and col. 8 lines 30-33 in Ryan and col. 8 lines 24-48 and Fig. 7, Refs. 700 & 710 in Rosich).

As to claim 67, Manning further discloses the step of maintaining a mode select signal to select a burst mode of operation (Col. 6 lines 14-34); receiving a stream of addresses and a cycling a second enabling signal (Fig. 2 /CAS); changing the mode select signal to select a pipelined mode of operation (col. 5 lines 43-50).

As to claim 68, Manning further discloses the steps of selecting a pipeline mode (col. 5 lines 43-49); select an external address only path when the pipeline mode is selected (col. 5 lines 43-49, "one access per cycle" and col. 3 lines 20-22 read on this limitation); and selecting an internal buffered external address path (col. 4 lines 23+ and col. 3 lines 20-22) and generating internal column address (col. 8 line 67) when the burst mode of operation is selected.

As to claims 63 and 69, Manning further discloses an external address only path for the pipeline mode (col. 5 lines 43-49, "one access per cycle" and col. 3 lines 20-22 read on this

limitation); an internal buffered external address path for the burst mode of operation (col. 3 lines 20-22, col. 4 lines 23+ & col. 8 line 67); and pipeline (col. 5 lines 41-50)/burst circuitry (col. 6 lines 14-26 and col. 7 lines 43-54) .

As to claim 64, Manning further discloses the operations are performed in a different order (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col. 6 lines 14+).

12. Claims 70-74 are rejected under 35 USC § 103(a) as being unpatentable over Manning, U.S. Patent 5,610,864 in view of Micron, 1996 DRAM Data Book, pp 1-3.

As to claim 70, Manning discloses a method for accessing an asynchronous DRAM (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16), comprising the steps of: switching between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 43-50); selecting an external data path (col. 3 lines 20-22, col. 4 lines 23+ & col. 8 line 67 and col. 5 lines 43-49); instructing the asynchronous DRAM a desired memory operation (Fig. 2 /WE); and performing the desired memory operation until terminated (Fig. 2 /WE, switching between read and write read on this limitation).

Although Manning discloses the step of switching between a burst and a pipelined mode of operation Manning does not specifically disclose switching between a burst and a pipelined mode of operation in the absence of a WCBR cycle.

However it is well known in the computer art that memory access is prohibited during the

WCBR cycle because the memory is being programmed during the WCBR cycle.

One skilled in the art would have recognizes that prohibiting the data access during WCBR (programming) cycle would preventing invalid data access thereby preventing a system crash.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the step of accessing data in the absence of a WCBR cycle of Micron in the invention of Manning because it would prevent invalid data access thereby preventing a system crash.

As to claim 71, Manning and Micron disclose the calms as the above claim 70. Manning further discloses selecting the external address data path (col. 3 lines 20-22, col. 4 lines 23+ & col. 8 line 67 and col. 5 lines 43-49) from a buffer when the act of switching switches to the burst EDO mode.

As to claim 72, Manning and Micron disclose the calms as the above claim 70. Manning further discloses the step of instructing the asynchronous DRAM the desired memory operation, wherein desired memory operation is selected from a group consisting of a read operation and a write operation (Fig. 2 /WE).

As to claim 73, Manning and Micron disclose the calms as the above claim 70. Manning

further discloses the step of obtaining an external column address so as to perform the desired memory operation, and wherein performing includes iterating the act of obtaining the external column address until terminated (col. 3 lines 20-22, col. 4 lines 23+ & col. 8 line 67 and col. 5 lines 43-49).

As to claim 74, Manning and Micron disclose the claims as the above claim 73. Manning further discloses the step of generating an internal column address so as to perform the desired memory operation, and wherein generating includes iterating the act of generating until terminated (col. 3 lines 20-22, col. 4 lines 23+ & col. 8 line 67 and col. 5 lines 43-49).

Response to Amendment

13. Applicant's arguments with respect to claims 36-39, 59-62, and 63-74 have been considered but are deemed to be persuasive.

Applicant's remarks on page 2 concerning the references not teaching switching between a burst mode and pipeline mode is not considered persuasive. Manning discloses this limitation (col. 5 lines 43-47 and col. 7 lines 44-55, "the current invention includes a pipelined architecture" and "switching between standard fast page mode (non-EDO) and burst mode" read on this limitation, in other words, Manning discloses switching between fast page pipeline and burst See also, Fig. 2 and col. 6 lines 14-22) since Manning discloses that the current invention include a pipelined architecture (col. 5 lines 43-49) which would increase accessing speed. Ryan also

discloses the step of switching between a burst mode and pipeline mode (col. 4 line 24- 28).

In response to applicant's argument that Ryan reference (USP 5,966,724) can not be used is not considered persuasive, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's argument that Ryan (USP 5,966,724) is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the modification of the reference would not change the operation of the reference being modified since it only extends teaching of selection between two modes and one skilled in the memory art would have recognizes that teachings of selecting between two modes in a memory would use in an asynchronous memory because it would allow put the memory in high data throughput by eliminating the set up time (abstract lines 8-9). Rosich also discloses claimed limitation (col. 8 lines 24-48 and RASL in Fig. 7, Ref. 700, page mode & 710, burst mode).

Applicant's remarks on page 3 concerning the references not teaching changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active

state. Rosich discloses changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state (col. 8 lines 24-48 and RASL in Fig. 7, Ref. 700, page mode & 710, burst mode) for the purpose of reducing memory access time and component latency by enabling the memory chip throughout the operations (col. 1 lines 21-31).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Rosich discloses a step of switching modes of operation including a step of maintaining a first enabling signal in active state (col. 8 lines 24-48 and RASL in Fig. 7, Ref. 700, page mode & 710, burst mode) for the purpose of reducing memory access time and component latency by enabling the memory chip throughout the operations (col. 1 lines 21-31). Therefore broadly written claims are disclosed by the references cited.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. 1996 DRAM Data Book, Micron, pp 1-2, 1-3, 5-75 and 7-62.
2. USP 4766431 (abstract).

15. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

16. Applicants are requested to number each line of each claim starting with line number one to provide easier communication in the future.

17. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

18. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

19. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can

normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

20. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051-2, (for formal communications intended for entry)

Or:

(703) 305-9731 (for informal or draft communications, please label
"PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

HK
Patent Examiner
January 25, 2001

